AMENDMENTS TO THE CLAIMS

1-51. (canceled)

52. A method of synchronizing a clock signal using a delay lock loop, comprising:

frequency dividing the clock signal to provide a divided signal;

coupling the divided signal to an input of a variable delay circuit, the variable delay circuit outputting a delayed signal;

comparing the divided signal to a phase of the delayed signal to generate a control signal; and

applying the control signal to the variable delay circuit to control its delay.

53. The method of claim 52, further comprising an initially fixing said control signal to a reset value.

54. The method of claim 53, wherein the reset value sets the variable delay circuit to a minimum setting.

55. The method of claim 52, wherein the variable delay circuit includes a propagation delay.

56. The method of claim 52, wherein the control signal comprises use of an integrator.

57. The method of claim 52, wherein the control signal comprises use of a charge pump.

58. The method of claim 52, wherein comparing the divided signal to a phase of the delayed signal to generate a control signal involves assessing the phase difference between the divided signal and the delayed signal.

59. The method of claim 52, wherein the method produces the delayed signal such that it is synchronized with reading or writing of data to and from a memory array.

60. The method of claim 59, further comprising coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal.

61. The method of claim 60, further comprising selecting one of the delayed representations to synchronize the reading and writing.

62. The method of claim 61, wherein selecting is accomplished by a multiplexer.

63. A method of locking a delay lock loop in synchronization with a clock signal, comprising:

initializing a variable delay circuit within the delay lock loop to a minimum delay value, wherein the output of the variable delay circuit is coupled to a feedback loop, and wherein delay of the variable delay circuit is controlled by a control signal generated by the feedback loop;

frequency dividing the clock signal and inputting it into the variable delay circuit; and

locking the frequency-divided clock signal by adjusting the control signal to the variable delay circuit.

64. The method of claim 63, further comprising coupling a frequency divider into the feedback loop after locking.

65. The method of claim 63, wherein the variable delay circuit includes a propagation delay.

66. The method of claim 63, wherein the feedback loop comprises a phase detector for comparing the phase difference between the clock signal and the output of the variable delay circuit.

67. The method of claim 66, further comprising an integrator coupled to the phase detector for producing the control signal.

68. The method of claim 63, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

69. The method of claim 68, further comprising coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal.

70. The method of claim 69, further comprising selecting one of the delayed representations to synchronize the reading and writing.

71. The method of claim 70, wherein selecting is accomplished by a multiplexer.

72. A delay lock loop circuit, comprising:

a variable delay circuit configured to receive a frequency divided version of the clock signal;

a phase detector for receiving as inputs (i) the output of the variable delay circuit and (ii) the frequency divided version of the clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.

73. The circuit of claim 72, wherein the variable delay circuit includes a propagation delay.

74. The circuit of claim 72, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal.

75. The circuit of claim 72, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

76. The circuit of claim 75, further comprising a vernier circuit coupled between the variable delay circuit and the phase detector for producing various delayed representations of the output of the variable delay circuit.

77. The circuit of claim 76, further comprising a multiplexer for selecting one of the delayed representations to synchronize the reading and writing.

78. The circuit of claim 72, further comprising a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal.

79. The circuit of claim 72, wherein the control signal is resettable to a minimum value.

80. A memory device accessible by a first clock signal, comprising:

a memory array accessible by a second clock signal; and

a delay lock loop for synchronizing the second clock signal with the first clock signal, comprising:

a variable delay circuit for producing the second clock signal, wherein the variable delay circuit is configured to receive a frequency divided version of the first clock signal;

a phase detector for receiving as inputs (i) either the second clock signal, and (ii) the frequency divided version of the first clock

signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.

81. A system, comprising:

a microprocessor for producing a first clock signal;

a memory device for receiving the first clock signal, the memory device comprising a memory array accessible by a second clock signal; and

a delay lock loop for synchronizing the second clock signal with the first clock signal, comprising:

a variable delay circuit for producing the second clock signal, wherein the variable delay circuit is configured to receive a frequency divided version of the first clock signal;

a phase detector for receiving as inputs (i) either the second clock signal, and (ii) the frequency divided version of the first clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.